AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1093] with the following amended paragraph:

[1093] As described above, for many memory arrays, and especially for a three-dimensional (3D) memory, utilizing depletion mode devices when erased and near depletion mode devices (i.e., around one volt V_T, such as, for example, 0.5 to 1.5V) when programmed has a great advantage in simplifying the layout complexity for each of the memory layers, as described herebelow. Moreover, utilizing near depletion mode devices when programmed reduces the voltages that need to be applied to the unselected word lines when reading a selected memory cell. The cell current can pass more easily through the string even if unselected memory cells are programmed. This voltage reduction is beneficial for reducing disturb effects during the many expected read cycles. For example, an unselected memory cell on an unselected NAND string which is erased could be slowly disturbed to a programmed ~~stated~~ state by higher voltages on the word lines.

Please replace paragraph [1111] with the following amended paragraph:

[1111] In various embodiments of the invention described herein, the memory cells may be comprised of semiconductor materials, as described in U.S. Patent 6,034,882 to Johnson et al., U.S. Patent 5,835,396 to Zhang, U.S. Patent Application Serial No. 09/560,626 by Knall, and U.S. Patent Application Serial No. 09/638,428 by Johnson, each of which are hereby incorporated by reference. Specifically an antifuse memory cell is preferred. Other types of memory arrays, such as MRAM and organic passive element arrays, may also be used. MRAM (magnetoresistive random access memory) is based on magnetic memory elements, such as a magnetic tunnel junction (MTJ). MRAM technology is described in "A ~~2556kb~~ 256kb 3.0V ~~1T1MTJ~~ 1T1MTJ Nonvolatile Magnetoresistive RAM" by Peter K. Naji et al., published in the Digest of Technical Papers of the 2001 IEEE International Solid-State Circuits Conference, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001 and pages 94-95, 404-405 of ISSCC 2001 Visual Supplement, both of which are hereby incorporated by reference. Certain passive element memory cells incorporate layers of organic materials including at least one layer that has a diode-like characteristic conduction and at least one organic material that changes conductivity with the application of an electric field. U.S.

Patent No. 6,055,180 to Gudensen et al. describes organic passive element arrays and is also hereby incorporated by reference. Memory cells comprising materials such as phase-change materials and amorphous solids can also be used. See U.S. Patent No. 5,751,012 to Wolstenholme et al. and U.S. Patent No. 4,646,266 to Ovshinsky et al., both of which are hereby incorporated by reference.

Please replace paragraph [1117] with the following amended paragraph:

[1117] It will be appreciated by one skilled in the art that any of several expressions may be equally well used when describing the operation of a circuit including the various signals and nodes within the circuit, and no subtle inferences should be read into varied usage within this description. Frequently logic signals are named in a fashion to convey which level is the active level. The schematic diagrams and accompanying description of the signals and nodes should in context be clear. As ~~use~~ used herein, two different voltages which are "substantially equal" to each other have respective values which are close enough to cause substantially the same effect under the context at issue. Such voltages may be assumed to fall within approximately 0.5 volts of each other, unless the context requires another value. For example, a passing voltage of 5 volts or 5.5 volts may cause substantially the same effect as compared to an inhibit bias voltage of 5 volts, and thus the 5.5 volt passing voltage may be considered to be substantially identical to the 5 volt inhibit voltage.